Amendments to the Claims

1. (*Currently Amended*) A method of powering an integrated circuit, said integrated circuit comprising a chip ~~(4)~~ within a package assembly ~~(6)~~, said chip comprising a plurality of logic circuits ~~(16, 18)~~, each of the logic circuits having at least one power input which should not receive a power voltage exceeding a predetermined maximum operating voltage, the method comprising the steps of:

[[-]] measuring ~~(in a step 98)~~ the power voltage supplied to the integrated circuit, and

[[-]] regulating ~~(in a step 96)~~ this power voltage in order to keep the difference between the measured voltage and a reference voltage as small as possible,

[[-]] wherein during the measuring step the power voltage is directly measured within the chip at the power input of at least one of the logic circuits, and

[[-]] wherein the method comprises the step of setting ~~(in a step 92)~~ the reference voltage such that the voltage supplied to the power input of at least one logic circuit of the chip is equal to the predetermined maximum operating voltage of this logic circuit.

2. (*Currently Amended*) The method according to claim 1, wherein during the measuring step ~~(in step 98)~~ the power voltage is measured within the chip directly at the power input of the logic circuit known to be the first to be damaged in the case of a power voltage increase on at least one power input lead of the integrated circuit.

3. (*Currently Amended*) The method according to claim 2, wherein during the measuring ~~(in step 98)~~ the power voltage is measured within the chip directly at the power input of the logic circuit known to be supplied with the highest power voltage available within the chip.

4. (*Currently Amended*) The method according to claim 1, wherein, during the measuring step ~~(in step 98)~~ the power voltage is measured within the chip directly at the power input of a first logic circuit, and wherein during the setting step, the reference voltage is set to the value of the predetermined maximum operating voltage of a second logic circuit known to be the first to be damaged in the case of a power

voltage increase on at least one power input lead of the integrated circuit minus a margin voltage representative of a voltage drop between the power inputs of the first and second logic circuits.

5. (*Currently Amended*) A powering system comprising:

[[-]] an integrated circuit ~~(2)~~ comprising a chip ~~(4)~~ within a package assembly ~~(6)~~, said chip comprising a plurality of logic circuits ~~(16, 18)~~, each of the logic circuits having at least one power input which should not receive a power voltage exceeding a predetermined maximum operating voltage, and the package comprising at least one power input lead ~~(8)~~,

[[-]] a power supply ~~(32)~~ to supply a power voltage to said at least one power input lead ~~(8)~~, said power supply being able to regulate the power voltage supplied in dependence on the difference between a reference voltage and a voltage measured at a sensing point ~~(61)~~,

[[-]] wherein the sensing point ~~(61)~~ is placed within the chip ~~(4)~~ of the integrated circuit at the power input of one of the logic circuits ~~(16)~~, and

[[-]] wherein the reference voltage is set so as to supply to the power input of at least one logic circuit a voltage equal to the predetermined maximum operating voltage of this logic circuit.

6. (*Currently Amended*) The system according to claim 5, wherein the sensing point ~~(61)~~ is placed at the power input of the logic circuit known to be the first to be damaged in the case of a power voltage increase on said at least one power input lead ~~(8)~~.

7. (*Currently Amended*) An integrated circuit comprising <u>comprising,</u>

a chip ~~(4)~~ within a package assembly ~~(6)~~, said chip comprising a plurality of logic circuits ~~(16, 18)~~, each of the logic circuits having at least one power input which should not receive a power voltage exceeding a predetermined maximum operating voltage, the package assembly being provided with a plurality of leads ~~(8, 5, 40, 54)~~ to be connected to an external circuit board, one of these leads ~~(54)~~ being a sensing lead to measure the voltage directly at a sensing point ~~(61)~~ within the chip and another lead being a power input lead ~~(8)~~, wherein the sensing point ~~(61)~~ is placed at the

power input of the logic circuit ~~(16)~~ known to be the first to be damaged in the case of a power voltage increase on the power input lead ~~(8)~~.